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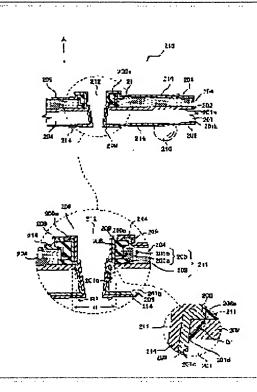
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## (54) SEMICONDUCTOR DEVICE AND ITS FABRICATING METHOD (57)Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device having a through hole penetrating an electrode pad and a semiconductor substrate in which sufficient insulation can be ensured between the electrode pad and the semiconductor substrate on the sidewall of the through hole.

SOLUTION: The semiconductor device comprises a silicon substrate 201 (semiconductor substrate), an element forming layer 202 (element) formed on one side 201a of the silicon substrate 201, an electrode pad 211 connected electrically with the element forming layer 202, a through hole 212 penetrating the electrode pad 221 and the silicon substrate 201, a via hole 209a made in an SiO2 film 209 (insulating film) on the electrode pad 221, and a wiring pattern 214 wherein the through hole 212 has diameter R2 at the part penetrating the silicon substrate 201 smaller than diameter R2 at the part penetrating the electrode pad 211.



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# Japanese Publication for Unexamined Patent Application No. 373895/2002 (Tokukai 2002-373895)

## A. Relevance of the Above-identified Document

This document has relevance to <u>claims 1 and 10</u> of the present application.

B. Translation of the Relevant Passages of the Document

See the attached English Abstract.

## [CLAIMS]

- 1. A semiconductor apparatus, comprising:
- a semiconductor substrate;
- a device formed on a surface of the semiconductor substrate:

an electrode pad which is (i) formed on the surface of the semiconductor substrate and (ii) electrically connected to the device;

a through-hole penetrating the electrode pad and the semiconductor substrate;

an insulating film formed at least on the other surface of the semiconductor substrate, an inside of the through-hole, and the electrode pad;

a via-hole formed in the insulating film on the electrode pad; and

a wiring-pattern electrically connecting the electrode pad to the other side of the semiconductor substrate via the through-hole and the via-hole,

#### wherein:

the through-hole through the semiconductor apparatus is larger in diameter than the through-hole through the electrode pad.

[0016]

## [MEANS FOR SOLVING THE PROBLEM]

aforementioned problem is solved semiconductor apparatus of the first invention. The semiconductor apparatus including (i) a semiconductor substrate, (ii) a device formed on a surface of the semiconductor substrate, (iii) an electrode pad which is (a) formed on the surface of the semiconductor substrate and (b) electrically connected to the device, (iv) a through-hole penetrating the electrode pad and the semiconductor substrate, (v) an insulating film formed at least on the other surface of the semiconductor substrate, an inside of the through-hole, and the electrode pad, (vi) a via-hole formed in the insulating film on the electrode pad, and (vii) a wiring-pattern electrically connecting the electrode pad to the other side of the semiconductor substrate via the through-hole and the via-hole. In the

semiconductor apparatus, a diameter of the through-hole in the semiconductor apparatus is larger than a diameter of the through-hole in the electrode pad.

[0044]

The via-hole 209a is formed on the electrode pad 211. The via-hole 209a under which the electrode pad 211 is provided electrically connects the electrode pad 211 to the wiring pattern 214. Note that an existent semiconductor device has the electrode pad 211, which is the electrode pad is not newly provided for the present invention. That is, in the present invention, the wiring pattern 214 is electrically connected to the existent electrode pad 211 unlike a conventional art, in which the wiring pattern 214 is connected to a via-electrode pad additionally provided. [0045]

The via-electrode does not need to be provided in the present invention because the via-hole 209a having a ring shape is formed along the aperture of the through-hole 212 as shown in Fig. 2(a). According to the via-hole 209a, sufficient space is ensured for electrical connection to the wiring pattern. On this account, the via-electrode does not need to be additionally provided unlike in the conventional art.

[0046]

In the conventional art, there is a problem that the via-electrode pad 110 (see Fig.15(b)) becomes larger in plane size as much as a space taken by the via-electrode pad 110. Furthermore, providing the via-electrode 110 in addition to the electrode pad 105 (see Fig.15(b)) means that a design of the existent semiconductor device has to change, accordingly, this imposes a great burden on a manufacturer (semiconductor manufacturing corporation) of a semiconductor apparatus.

[0047]

On the contrary, the present invention does not need the via-electrode pad, thereby solving the aforementioned problems. Note that the plane shape of the electrode pad 211 is substantially square approximately  $100\mu m$  on a side, as shown in Fig.2(a). However, the plane shape and the size of the electrode pad 211 are not limited to this, and may be arbitrarily set depending on circumstances. Furthermore, the via-hole 209a has a width of approximately  $5\mu m$  through  $10\mu m$ , but the width thereof is not limited to this.

[0048]

Alternatively, instead of the ring-shaped via-hole 209a shown in Fig. 2(a), the same effect can be obtained by providing the circular via-hole 209a arranged as shown in Fig. 2(b) through Fig. 2(d). Fig. 2(b) illustrates that an

arc-shaped via-hole 209a is formed along the aperture of the through hole 212. The number of the arc-shaped 209a is not limited to one but may be more than one as shown in Fig.2(c).

[0049]

Fig. 2(d) illustrates that a plurality of dot-shaped via-hole 209a is formed along the aperture of the through-hole 212. However, the shape of the via-hole is not limited to this. Note that the aforementioned advantage of the present invention can be obtained as long as the via-hole 209a is formed along the through-hole 212.

[0050]

also that in case where providing the via-electrode pad as in the conventional art does not cause any problem, the via-hole 209a does not need to be formed along the aperture of the through-hole 212. See Fig.1 again. As indicated by the circle drawn in broken lines, the through-hole 212 is defined by the first aperture 208 and the second aperture 201c. The first aperture 208 is the part penetrating the electrode pad 211, and the second aperture 201c is the part penetrating the silicon substrate 201.

[0051]

In the present invention, the diameter R1 of the first

aperture 208 is bigger than the diameter R2 of the second aperture 201c. Specifically, R1 is approximately 50µm through 70µm, and R2, which should be smaller than R1, is approximately 25µm through 50µm. Note that the present invention is not limited to the aforementioned numeric values as long as R1 is bigger than R2. According to the arrangement, distance D1 (see the circle, drawn in broken lines, in the right bottom in Fig.1) between an aperture edge 208a of the first aperture 208 and an aperture edge 201d of the second aperture 201c can be longer than in the arrangement in which the diameter R1 and R2 has the same length. This ensures sufficient insulation between the electrode pad 211 and the silicon substrate 201 in the side-surface of the through-hole 212.

[0066]

Subsequently, as shown in Fig.6(d), a second photo resist 207 is formed on the respective exposed areas of the passivation layer 204 and the electrode pad 211. After that, the photo resist 207 is exposed to light and developed, thereby forming a second resist aperture 207a through which the electrode pad 211 is bared. After that, as shown in Fig. 6(e), and the electrode pad 211 is patterned by using the photo resist 207 as an etching mask, after that, a first aperture 208 is formed on the

electrode pad 211. In this case, the etching is carried out by utilizing, for example, the chemical etching method or the plasma etching method. Note that the diameter R1 of the first aperture is approximately  $50\mu m$  through  $70\mu m$ , but may be arbitrarily changed depending on the diameter of the electrode pad 211.

[0067]

Subsequently, as shown in Fig. 7(a), the other surface 201b of the silicon substrate 201 is grinded so as to thin the silicon substrate 201 until the silicon substrate 201 has a thickness of approximately  $50\mu m$  through  $150\mu m$ . This step gives such an advantage that the semiconductor apparatus to be formed will be thinner. However, in case where there is no need to make the semiconductor apparatus thinner, this step may be omitted. Next, as shown in Fig.7(b), laser beam, whose diameter is smaller than the diameter R1 of the first aperture 208, is irradiated passing through the first aperture 208. The laser beam may be the UV laser beam, the YAG laser beam, the excimer laser beam, or the like. An area where the laser beam is irradiated is evaporated, thereby forming a second aperture 201c on the silicon substrate 201. The diameter R2 of the second aperture 201c is approximately  $25\mu m$  through  $50\mu m$ . The first aperture 208 and the second aperture 201c define the through-hole 212.

[0068]

As described above, after the first aperture 208 is formed, the laser beam whose diameter is smaller than the diameter R1 of the first aperture 208 is irradiated. This prevents the laser beam from touching the first aperture 208 thereby evaporating the material (aluminum and copper) of the electrode pad 211. Because evaporation of the material is prevented, lowering the risk that the silicon substrate 201 and the electrode pad 211 are electrically connected by the material evaporated and adhered to the side-surface of the through hole.

Further, according to the aforementioned step, the diameter R1 of the first aperture 208 is larger than the diameter R2 of the second aperture 201c. As explained above, this ensures sufficient electrical insulation between the electrode pad 211 and the silicon substrate 201. Furthermore, because the silicon substrate 201 is thinned in the step shown in Fig.7(a) before the second aperture 201c is formed, the second aperture 201c can be formed by a laser beam irradiation in a short time. This decreases a thermal damage imposed on the silicon substrate 201 due to the laser beam irradiation.

[0070]

Further, because depth to process by the laser beam is

shallow, the amount of the silicon evaporated by the laser beam irradiation is decreased, whereby, the amount of the silicon which is evaporated and adhered to the inside of the through hole 212 is decreased. On this account, the through-hole 212 can be cleanly formed. Note that, in case where the thermal damage or the adhesion of the silicon onto the inside of the through-hole 212 cause no problem, the step shown in Fig. 7(a) – the step for thinning the silicon substrate 201 – may be omitted. [0071]

Incidentally, the second aperture 201c is in a taper shape as shown in the figure because the laser beam is not irradiated in parallel but condensed in one point by utilizing a condenser lens. However, this does not mean that the shape of the second aperture 201 is limited to such taper shape. For example, even if the second aperture is in a straight shape, the same effect of the present invention can be obtained.

[0072]

Further, the laser beam may be irradiated to the other surface 201b of the silicon substrate 201 so as to form the second aperture 201c, instead of irradiating the laser beam passing through the first aperture 208 as described above. In this arrangement, it is also possible to prevent the silicon evaporated by the laser beam irradiation from

adhering to the electrode pad 211. Furthermore, the step shown in Fig. 12 may be carried out between the step shown in Fig. 7(a) and the step shown in Fig. 7(b). In this step, a protective film 216 such as a SiO<sub>2</sub> film or the like is formed on the passivation film 204, the electrode 211, the side-surface of the first aperture 208, and the device-mounting layer 202. In case where a debris and a valley is formed during the laser irradiation shown in Fig. 7(b), cleaning (such as plasma-cleaning or chemical wash) is carried out. By forming the protective film 216, it is possible to prevent damage, during the cleaning, on the electrode pad 211 and the passivation layer 204.